IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In RE:

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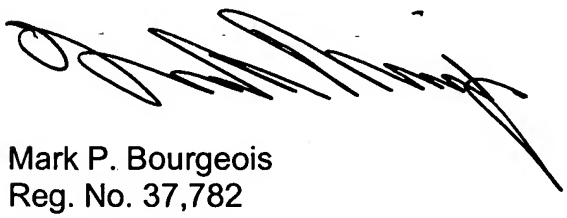
For:	Micro Machined Semi-Conductor Package
Inventor:	Langhorn
Atty. Docket no.:	CTS-2287
Group Art Unit:	2811
Examiner:	Gebremariam
Confirmation no.:	5009

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

This is in response to the Notice of Appeal filed November 12, 2004. The Commissioner is hereby authorized to charge payment of all fees associated with this communication or credit any overpayment to Deposit Account No. 03-1677.

Enclosed are triplicate copies of the appeal brief as required.

Respectfully submitted,



Mark P. Bourgeois
Reg. No. 37,782

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APPEAL BRIEF

Real Party in interest

The real party in interest in the present appeal brief is CTS Corporation, the assignee of the present patent application.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 25-28 are pending. Claims 25-28 were finally rejected under 35 U.S.C. 103(a) as being unpatentable over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190). The final rejection of claims 25-28 is being appealed.

Status of Amendments

There are no amendments that have not been entered.

Summary of Invention

The invention is a multilayered ceramic package having a cavity with structural supports that is bonded to a micro-machined semiconductor device and is best depicted in figure 1. Figure 1 shows a cross sectional view of an embodiment of a micro-machined semiconductor package. The preferred embodiment of the invention is

exemplified in claim 25, which recites a semiconductor package that includes a planar low temperature co-fired ceramic substrate 12 having a first 16 and second layer 14 mounted adjacent each other. The first layer has a first surface 16B and the second layer has a second surface 14A. Support for this is found in the specification on page 5, lines 6-10 and in figure 1.

A micro-machined semiconductor device 40 is located adjacent the first surface 16B. The micro-machined semiconductor device has a plurality of first pads 46 and an active central area 42. Support for this is found in the specification on page 6, lines 19-22 and page 7, lines 1-2 and in figure 1.

A plurality of ball pads 22 are located on the second surface 14A. Support for this is found in the specification on page 5, lines 14-16 and in figure 1.

A plurality of second pads 26 are located on the first surface 16B. Support for this is found in the specification on page 6, lines 14-15 and in figure 1.

A plurality of vias 20 extend through the substrate between the first and second surfaces. The vias are connected to the ball pads and to the first pads. Support for this is found in the specification on page 5, lines 10-14 and in figure 1.

A reflowed solder joint 32 is located between the first 46 and second pads 26 for electrically connecting the substrate to the semiconductor device. The reflowed solder joint 32 is formed from a first reflowed solder paste. Support for this is found in the specification on page 6, lines 14-18 and in figure 1.

A solder seal ring 27 is located between the micro-machined semiconductor device 40 and the first surface 16B around an outer perimeter of the substrate for making a hermetic seal between the micro-machined semiconductor device and the

substrate. Support for this is found in the specification on page 6, lines 7-13 and in figure 1.

A plurality of ultrasonically deposited wire bond bumps 60 are located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface during reflow of the solder joint 32. The wire bond bumps 60 further spacing the micro-machined semiconductor device from the first surface. The wire bond bumps 60 are further arranged around the active area. The wire bond bumps are formed from a metal. Support for this is found in the specification on page 7, lines 7-20 and in figure 1.

A plurality of solder spheres 18 are mounted to the ball pads 22 by a second reflowed solder paste 23. Support for this is found in the specification on page 5, lines 16-19 and in figure 1.

Issues

Issue 1 - Whether claim 25 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Issue 2 - Whether claim 26 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Issue 3 - Whether claim 27 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Issue 4 - Whether claim 28 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Grouping of Claims

For each ground of rejection, which appellant contests herein, which applies to more than one claim, such additional claims, to the extent separately identified and argued below, do not stand or fall together.

Argument

Issue 1 - Whether claim 25 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Independent claim 25 recites a semiconductor package that has a low temperature co-fired ceramic substrate with a first and second layer. The first layer has a first surface and the second layer has a second surface. A micro-machined semiconductor device is located adjacent the first surface and has a plurality of first pads and an active central area. Several ball pads are located on the second surface. Several second pads are located on the first surface. Several vias extend through the substrate between the first and second surfaces. The vias are connected to the ball pads and to the first pads. A reflowed solder joint is located between the first and second pads. A solder seal ring is located between the micro-machined semiconductor device and the first surface. Several metal wire bond bumps are located between the micro-machined semiconductor device and the first surface. Several solder spheres are mounted to the ball pads by a second reflowed solder paste.

The cited Hinds reference EP 1057779 A2 discloses a flip chip package for micro-machined semiconductors. The Hinds device uses an extra layer of ceramic 30 in order to space the semiconductor device 40 from the substrate 12.

The cited Kainuma reference US 6,483,190 discloses a semiconductor chip 100 that is attached to a circuit board 120 using stud bumps 117. All signal connections are made using stud bumps 117.

None of the cited references show or suggest a rigid support bump that is used during solder reflow. There is no disclosure in Hinds or Kainuma of supporting the MEMS device during solder reflow in order to maintain the proper distance between the MEMS device and the substrate.

There is no suggestion in Hinds to combine the references in the manner shown to utilize ultrasonically deposited gold bond bumps. As the court of Appeals for the Federal Circuit has set forth, even if a prior art reference could be modified to construct an applicant's invention, the modification is not obvious unless there is a suggestion in the prior art. *In re Laskowski*, 10 USPQ2d 1397, 1398 (Fed. Cir. 1989). There is no suggestion to modify Hinds in the manner suggested.

Assuming that Hinds and Kainuma could be properly combined, the combination would require making all of the electrical connections using stud bumps. The combined product would not be able to use a solder seal ring to provide a hermetic seal and would require the use of three layers of ceramic.

The examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. This burden can be satisfied only by showing some objective teaching in the prior art or that knowledge generally available to one of

ordinary skill in the art would lead that individual to combine the relevant teachings of the references. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988) (citing *In re Lalu*, 747, F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1984). A rejection based upon 35 U.S.C. 103 must rest on a factual basis, with the facts being interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, a factual basis for the rejection must be advanced. Because of doubt that an invention is patentable, an examiner may not resort to speculation, unfound assumptions or hindsight reconstruction to supply deficiencies in the factual basis. *In re Warner*, 379 F.2d 1016-1017, 154 USPQ 173(CCPA 1967). It is respectfully submitted that a factual basis for the rejection has not been supplied and that the rejection relies upon hindsight reconstruction of the invention.

Applicant respectfully submits that claim 25 is patentably distinguishable over the art of record and that the 103 rejection be withdrawn.

Issue 2 - Whether claim 26 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Dependent claim 26 recites a plurality of circuit lines that are located on the first surface. The circuit lines are connected between the vias and the second pads.

For the same reasons advanced in issue 1 for claim 25, claim 26 is patentable over the art of record. Since the teachings relied upon are not present in Hinds or Kainuma, the combination fails to disclose the invention of claim 26. Applicant

respectfully submits that claim 26 is patentably distinguishable over the art of record and that the 103 rejection be withdrawn.

Issue 3 - Whether claim 27 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

Dependent claim 27 recites the substrate does not have cavity.

Hinds has a cavity. If the combination of Hinds and Kainuma were made, it would require a cavity in order to provide a hermetic seal. The combination would lack having a metal ring on the chip that can be soldered to form a hermetic seal. The semiconductor device of Kainuma does not teach having a solderalbe metal ring.

Applicant respectfully submits that claim 27 is patentably distinguishable over the art of record and that the 103 rejection be withdrawn.

Issue 4 - Whether claim 28 is patentable under 35 USC 103 over Hinds (EP 1057779 A2) in view of Kainuma (US 6,483,190)?

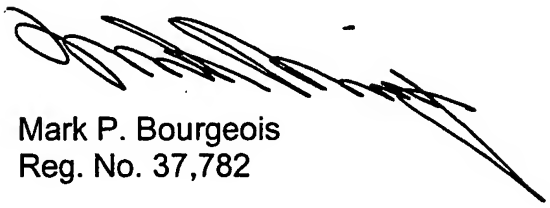
Dependent claim 28 recites the wire bond bumps are formed from either gold or an alloy of gold.

For the same reasons advanced in issue 1 for claim 25, claim 28 is patentable over the art of record. Since the teachings relied upon are not present in Hinds or Kainuma, the combination fails to disclose the invention of claim 28. Applicant respectfully submits that claim 28 is patentably distinguishable over the art of record and that the 103 rejection be withdrawn.

Conclusion

For the extensive reasons advanced above, Appellant respectfully contends that each claim is patentable. Accordingly, reversal of all rejections is courteously solicited.

Respectfully submitted,



Mark P. Bourgeois
Reg. No. 37,782

Appendix

The claims involved in the appeal follow below:

25. A semiconductor package comprising:

a planar low temperature co-fired ceramic substrate having a first and second layer mounted adjacent each other, the first layer having a first surface and the second layer having a second surface;

a micro-machined semiconductor device located adjacent the first surface, the micro-machined semiconductor device having a plurality of first pads and an active central area;

a plurality of ball pads located on the second surface;

a plurality of second pads located on the first surface;

a plurality of vias, extending through the substrate between the first and second surfaces, the vias connected to the ball pads and to the first pads;

a reflowed solder joint located between the first and second pads for electrically connecting the substrate to the semiconductor device, the reflowed solder joint formed from a first reflowed solder paste;

a solder seal ring, located between the micro-machined semiconductor device and the first surface around an outer perimeter of the substrate for making a hermetic seal between the micro-machined semiconductor device and the substrate;

a plurality of ultrasonically deposited wire bond bumps located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined

semiconductor device from contacting the first surface during reflow of the solder joint, the wire bond bumps further spacing the micro-machined semiconductor device from the first surface, the wire bond bumps further arranged around the active area, the wire bond bumps formed from a metal; and

a plurality of solder spheres mounted to the ball pads by a second reflowed solder paste.

26. The semiconductor package according to claim 25, wherein a plurality of circuit lines are located on the first surface, the circuit lines connected between the vias and the second pads.

27. The semiconductor package according to claim 25, wherein the substrate does not have cavity.

28. The semiconductor package according to claim 25, wherein the wire bond bumps are formed from either gold or an alloy of gold.